Abstract

A circuit isolation technique that uses implanted ions in embedded portions of a wafer substrate to lower the resistance of the substrate under circuits formed on the wafer or portions of circuits formed on the wafer to prevent the flow of injected currents across the substrate. The embedded ions provide low resistance regions that allow injected currents from a circuit to flow directly to a ground potential in the same circuit rather than flowing across the substrate to other circuits. High energy implantation processes on the order of 1 MeV to 3 MeVs can be used to implant the ions in embedded regions. Multiple energy levels can be used to provide thick embedded layers either prior to or after application of an epitaxial layer. Various masking materials can be used to mask the isolation regions during the implantation process, including hard masking materials such as silicon dioxide or silicon nitride, poly-silicon or an amorphous silicon layer, and a photoresist layer. Additive materials can be used in one or more of the masking layers to increase the absorption characteristics of the high energy ions. Separate physical masks can be used to block the implantation of ions.